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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,243	07/17/2003	Ashish D. Alawani	0140111	2882

25700 7590 08/27/2008

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EXAMINER	
LEVI, DAMEON E	
ART UNIT	PAPER NUMBER
2841	
MAIL DATE	DELIVERY MODE
08/27/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/623,243	ALAWANI ET AL.	
	Examiner	Art Unit	
	DAMEON E. LEVI	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06/03/2008(Amendment)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,9-14,16,18 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9-14,16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 9-14, 16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al US Patent 6521997 in view of Myers et al US Patent 6693239.

Regarding claim 1, Huang et al discloses a module comprising:

a surface mount component(elements 15,15' Figs 1-4) situated over a laminate circuit board(elements 10,1' Figs 1-4) the surface mount component comprising a first terminal(elements 150 Figs 1-4) and a second terminal(elements 151 Figs 1-4);

a first and a second pad situated on the laminate circuit board, (elements 12, Figs 1-4) the first pad being connected to the first terminal and the second pad being connected to the second terminal(elements 12,150,151, Figs 1-4),

a solder mask trench (elements 13, Figs 1-4) situated underneath the surface mount component, wherein the solder mask trench is situated over a top surface of the laminate circuit board, wherein a solder mask (elements 11, Figs 1-4) uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench(elements 11,13, Figs 1-4),

wherein a bottom surface of the surface mount component and the top surface of the laminate circuit board form a moldable gap (elements 152, 16, Figs 1-4) the moldable gap including the solder mask trench(elements 13,16 Figs 1-4), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound underneath the surface mount component, and wherein the solder mask trench is filled with the molding compound (see column 3, lines 37-50).

Huang et al does not expressly disclose

- wherein the overmolded module is an MCM, or,
- wherein said solder mask trench minimizes void formation in said molding compound underneath said surface mount component in said MCM.

Myers et al discloses a device wherein an overmolded module is an MCM(elements 30 Figs 4-10, Abstract) ,and, wherein said solder mask trench minimizes void formation in said molding compound underneath said surface mount component in said MCM(column 3, lines 1-7).

Accordingly, it would have been obvious to one skilled in the art at the time the invention was made to have included an MCM, as well as, to provide for minimizing void formation as taught by Myers et al in the device as taught by Huang et al as MCMs are commonplace in the art, and are commonly molded in order to provide for good thermal dissipation, as well as, to environmentally seal the chips(see Myers et al column 3, lines 8-15).

Regarding claim 3, Huang et al discloses wherein the moldable gap is filled with the molding compound(see column 3, lines 37-50).

Regarding claim 4, Huang et al discloses further comprising an overmold(elements 17 Figs 1-4), the overmold being situated over the surface mount component.

Regarding claim 5, Huang et al discloses wherein the surface mount component is selected from the group consisting of a resistor, a capacitor, an inductor, a diplexer, a diode, and a SAW filter (elements 15, Figs 1-4)

Regarding claim 6, Huang et al discloses wherein the moldable gap has a height of between approximately 45.0 micrometers and 65.0 micrometers (elements 16, Figs 1-4).

Regarding claim 9, Huang et al discloses a module comprising:

a surface mount component(elements 15,15' Figs 1-4) situated over a laminate circuit board(elements 10,1', Figs 1-4), the surface mount component comprising a first terminal and a second terminal(elements 151,152 Figs 1-4); a first and a second pad situated on the laminate circuit board(elements 15, Figs 1-4) , the first pad being connected to the first terminal and the second pad being connected to the second terminal, (elements 151,152,12 Figs 1-4);

a moldable gap(elements 16, Figs 1-4) situated underneath the surface mount component, the moldable gap comprising a solder mask trench (elements 13, Figs 1-4), wherein the solder mask trench is situated over a top surface of the laminate circuit board (elements 11, 10, Figs 1-3), wherein a solder mask (elements 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench(elements 11,13, Figs 1-4), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound

underneath the surface mount component, and wherein the solder mask trench is filled with the molding compound (see column 3, lines 37-50)

Huang et al does not expressly disclose

- wherein the overmolded module is an MCM, or,
- wherein said solder mask trench minimizes void formation in said molding compound underneath said surface mount component in said MCM.

Myers et al discloses a device wherein an overmolded module is an MCM(elements 30 Figs 4-10, Abstract) ,and, wherein said solder mask trench minimizes void formation in said molding compound underneath said surface mount component in said MCM(column 3, lines1-7).

Accordingly, it would have been obvious to one skilled in the art at the time the invention was made to have included an MCM, as well as, to provide for minimizing void formation as taught by Myers et al in the device as taught by Huang et al as MCMs are commonplace in the art, and are commonly molded in order to provide for good thermal dissipation, as well as, to environmentally seal the chips(see Myers et al column 3, lines 8-15).

Regarding claim 10, Huang et al discloses wherein the moldable gap is filled with the molding compound(see column 3, lines 37-50).

Regarding claim 11, Huang et al discloses further comprising an overmold(elements 17, Figs 1-4), the overmold being situated over the surface mount component.

Regarding claim 12, Huang et al discloses wherein the overmold comprises the molding compound (elements 17, Figs 1-4 ,column 3, lines 37-50).

Regarding claim 13,Huang et al discloses wherein the moldable gap has a height of between approximately 45.0 micrometers and 65.0 micrometers(elements 16, Figs 1-4)

Regarding claim 14, Huang et al discloses wherein the surface mount component is selected from the group consisting of a resistor, a capacitor, an inductor, a diplexer, a diode, and a SAW filter (elements 15, Figs 1-4).

Regarding claim 16, Huang et al discloses a module comprising:

a surface mount device(elements 15, Figs 1-4) situated over a laminate circuit board(elements 10,1', Figs 1-4), the surface mount device comprising a plurality of terminals(elements 151,152, Figs 1-4);a plurality of pads situated on the laminate circuit board(elements 12, Figs 1-4), each of the plurality of pads being connected to a respective one of the plurality of terminals(elements 151,152,12, Figs 1-4);

a solder mask trench(elements 13, Figs 1-4) situated underneath the surface mount device, wherein the solder mask trench is situated over a top surface of the laminate circuit board(elements 13, 10, Figs 1-4), wherein the moldable gap and the solder mask trench facilitate a flow of a molding compound underneath the surface mount component(elements 34,26,32 Figs 1-3) , and wherein a solder mask (elements 11, Figs 1-4)uniformly covers said top surface of said laminate circuit board, and wherein said solder mask does not cover said solder mask trench(elements 13, 11, Figs 1-4) wherein the solder mask trench is filled with the molding compound (column 3, lines 37-50).

Huang et al does not expressly disclose

- wherein the overmolded module is an MCM, or,

- wherein said solder mask trench minimizes void formation in said molding compound underneath said surface mount component in said MCM.

Myers et al discloses a device wherein an overmolded module is an MCM(elements 30 Figs 4-10, Abstract) ,and, wherein said solder mask trench minimizes void formation in said molding compound underneath said surface mount component in said MCM(column 3, lines1-7).

Accordingly, it would have been obvious to one skilled in the art at the time the invention was made to have included an MCM, as well as, to provide for minimizing void formation as taught by Myers et al in the device as taught by Huang et al as MCMs are commonplace in the art, and are commonly molded in order to provide for good thermal dissipation, as well as, to environmentally seal the chips(see Myers et al column 3, lines 8-15).

Regarding claim 18, Huang et al discloses wherein the surface mount device is a leadless surface mount device (elements 15, Figs 1-4).

Regarding claim 19, Huang et al discloses wherein the surface mount device comprises at least one component, the at least one component being selected from the group consisting of an active component and a passive component (elements 15, Figs 1-4).

Response to Arguments

Applicant's arguments filed 06/03/2008 have been fully considered but they are not persuasive. Applicants argue that the prior art fails to disclose or suggest an

ovennolded module including a solder mask trench that is situated over a top surface of a laminate circuit board, where a solder mask uniformly covers the top surface of the laminate circuit board, where the overmolded module is an MCM, and where the solder mask trench minimizes void formation in the molding compound underneath the surface mount component in the MCM, as specified in amended independent claims 1, 9, and 16.

In response the Office contends that the elements of the claimed invention are seen as being taught or suggested in the prior art as indicated in the rejections above. Furthermore, Myers et al teaches minimizing void formation underneath surface mount components(see Abstract, see column 3, lines 1-7).

It is the position of the Office, that one skilled in the art, given the teachings of Huang, in combination with, Myers et al, would have been reasonably apprised or the features of the claimed invention.

This rejection is maintained by the Office.

THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAMEON E. LEVI whose telephone number is (571)272-2105. The examiner can normally be reached on Mon.-Thurs. (9:00 - 5:00) IFP, Fridays Telework.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on (571) 272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeremy C. Norris/
Primary Examiner, Art Unit 2841

Dameon E Levi
Examiner
Art Unit 2841

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